CCSL COMPOSITE DATA SHEET

COMPATIBLE CURRENT SINKING LOGIC

-55°C TO +125°C TEMPERATURE RANGE

CCSL LOADING RULES

The first step towards realization of a compatable logic family is to establish optimized input-output logic levels. These levels. determine the noise immunity for all the elements, as well as the basis for system interfacing.

Fairchild CCSL loading rules guarantee the optimum logic levels over the full military temperature range of -55°C to +125°C with V_{CC} supply within the range of 5V ± 0.5V. These same logic levels, as well as the input load and output drive factors are also guaranteed over the temperature range of -20°C to +100°C, for all CCSL elements. These guaranteed levels are:

Low level output voltage (V_{OL}) = 0.4V
High level output voltage (V_{OH}) = 2.5V
Low level input voltage (V_{IL}) = 0.7V
High level input voltage (V_{IH}) = 2.1V

Noise immunity is derived from the above numbers according to the following equations.

1. High level noise immunity = $V_{OH} - V_{IH}$
2. Low level noise immunity = $V_{IL} - V_{OL}$

Once the logic levels and DC noise margins are established, interfacing rules can be resolved. To simplify input loading and output drive capability, load factors and drive factors were assigned to each element.

These factors are written as a ratio, but are not defined as an arithmetic ratio. The numerator can be added or subtracted independent of the denominator and vice versa. This ratio form was chosen for convenient loading rule analysis.

$$\text{Load Factor} \equiv \frac{\text{High Level Load Factor}}{\text{Low Level Load Factor}} \quad \text{(Shown as ratio on inputs to circuits)}$$

$$\text{Drive Factor} \equiv \frac{\text{High Level Drive Factor}}{\text{Low Level Drive Factor}} \quad \text{(Shown as ratio on outputs of circuits)}$$

Where:

High Level Load Factor = Input current drawn into the inputs, during the High Input Level State.
Low Level Load Factor = Input current drawn out of the input during the Low Input Level State.
High Level Drive Factor = Ability of the output to supply current out of the output during the High Output Level State.
Low Level Drive Factor = Ability of the output to sink current into the output during the Low Output Level State.

A necessary condition is that the High Level Drive Factor must be equal to or greater than the sum of the Driven High Level Load Factors and the Low Level Drive Factor must be equal to or greater than the sum of the Driven Low Level Load Factors. Both High Level Drive and Load factors and Low Level Drive and Load factors must be considered if efficient interfacing is to be accomplished.

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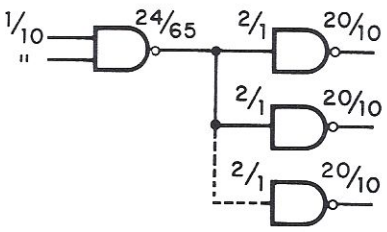
The load factors given are based on worst case conditions at both -55°C and +125°C. Input Low Level Load Factors are guaranteed with the Low Level Output Voltage (V_{OL}) applied to the inputs. Input High Level Load Factors are tested with arbitrarily selected voltages much higher than the V_{OH} value.

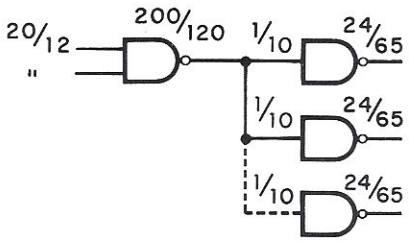
If the temperature range is restricted to -40°C to +110°C or the V_{CC} range to 4.75 to 5.25V, a 10% increase in drive factors may be used.

Examples: A.



(1) DTuL Gate (6K pullup) driving LPDTL Gates

B.



(2) TTL gate driving DTL Gates

Example A

Maximum load = 12 LPDTL gates. Limited by the high level drive capabilities. In this case the Low Level Load is only 12, and the drive capability is 65. Reference to the curves shown in Figure 1, will show this node to have a maximum V_{OL} = 100mV and therefore a worst case Low level noise immunity of 0.6 volts.

Example B

Maximum load - 12 DTL gates, limited by low level drive capabilities. Here the high level load = 12 and the drive capability is 200.

LIMITED LOADING APPLICATIONS

The curves shown in Figures 1, and 2 show improvements in the low level noise margin for TTL and DTμL. DTμL is shown with 6K or 2K pullup resistors.

Example: A TTL gate type output can drive a maximum of 120 low level loads and meet a guaranteed V_{OL} of 0.40 volts. If, however, this same output is only driving 50 low level loads, the worst case V_{OL} at that output would be 0.20 volts and the worst case low level noise immunity would be 0.50 volts.

Figure 2 shows similar low level curves for the TTL and DTμL Buffers.

Figure 3 shows the increase of V_{OH} of a DTμL output high level if the high level loads are less than the maximum specified in the CCSL loading rules. This drive is determined by using a -30% tolerence resistor and is guaranteed by D.C. testing.

Figure 4 shows changes in V_{OH} for DTμL devices which have 2K pullup resistor. The test point guarantees a V_{OH} 4.0 volts with 24 high level loads being driven. The increased number of loads which can be driven and still meet the CCSL V_{OH} of 2.5 volts is based on a worst case maximum tolerance pullup resistor as determined by D.C. testing. If less than 24 high level loads are driven, the increase in V_{OH} is determined by the worst case minimum tolerance pullup resistor.

TTL and LPDTμL devices having active pullups are relatively immune to changes in the high level loads. Their V_{OH} level is primarily set by being $2V_{BE}$'s below V_{CC}.

SPECIAL APPLICATIONS

When using the DTμL 9944 element, the following currents represent unit loads, and must be considered when choosing different external collector resistors.

		-55 C	+25 C	-125 C
V_{CC} = 4.5V	High Level	3μA	3μA	5μA
	Low Level	.121mA	Not worst case	Not worst case
V_{CC} = 5.5V	High Level	Not worst case	Not worst case	Not worst case
	Lower Level	.151mA	.154mA	.146mA

"WIRED OR" APPLICATIONS

For elements 9930, 9962, 9946 and 9936 add 24 to the High Level Drive Factor and subtract 9 from the Low Level Drive Factor for each added gate.

For elements 9041, 9043, 9046 and 9048 using one internal 15Ω pull-up resistor the High Level Drive Factor becomes 14 and the Low Level Drive Factor becomes 7. Subtract 2 from the High Level Drive Factor for each added gate.

Note 1

If the minimum temperature is limited to -30°C, the Low Level Drive Factor is 12.

CCSL INPUT LOAD & DRIVE FACTORS

QUAD 2-INPUT NAND GATES

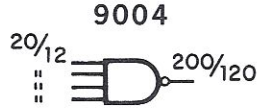
TRIPLE 3-INPUT NAND GATES

*See Note 1

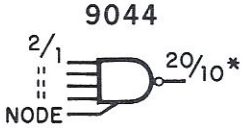
CCSL INPUT LOAD & DRIVE FACTORS

DUAL 4-INPUT NAND GATES

9004



9044



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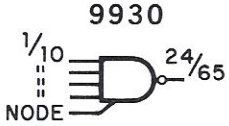

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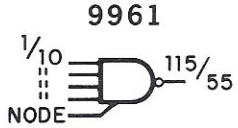
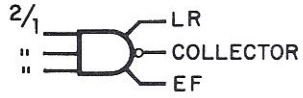


DUAL 3-INPUT NAND GATES

9041



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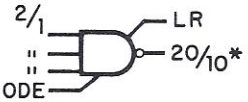


LR=LOAD RESISTOR OUTPUT, EF=EMITTER FOLLOWER OUTPUT

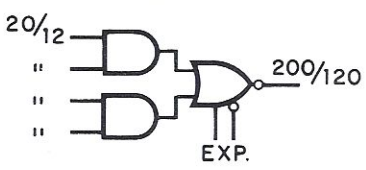
3 & 4-INPUT NAND GATES

9043

LR=LOAD RESISTOR OUTPUT

DUAL AND/NOR FUNCTION

9005



EIGHT-INPUT NAND GATE

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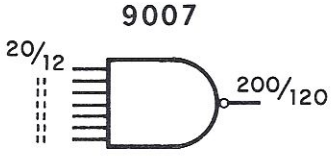


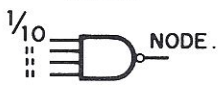
*See Note 1

CCSL INPUT LOAD & DRIVE FACTORS

DUAL 4-INPUT EXPANDERS

9006

9933



HEX INVERTERS

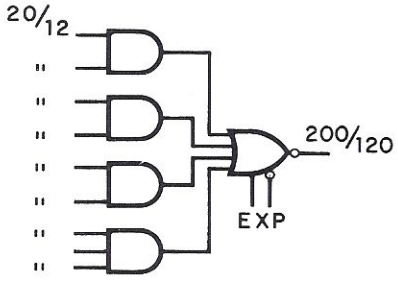
9935

9936

9937

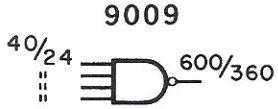
2-2-2-3-INPUT AND/NOR FUNCTION

9008



DUAL 4-INPUT BUFFERS

9009



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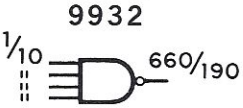


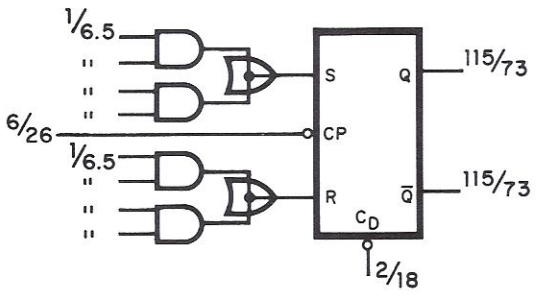
DUAL 4-INPUT DRIVER

9944

CCSL INPUT LOAD & DRIVE FACTORS

R-S FLIP-FLOPS

9111



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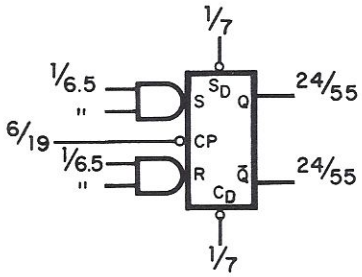

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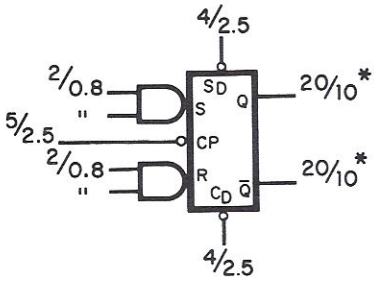

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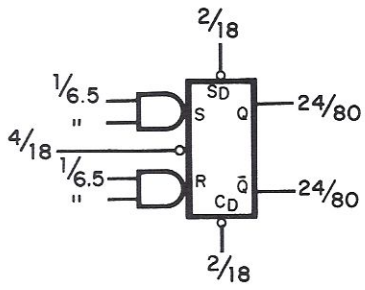

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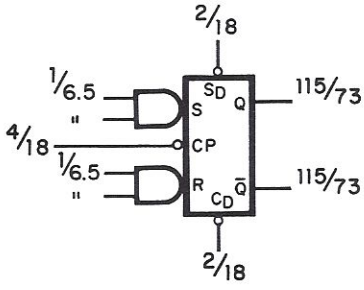
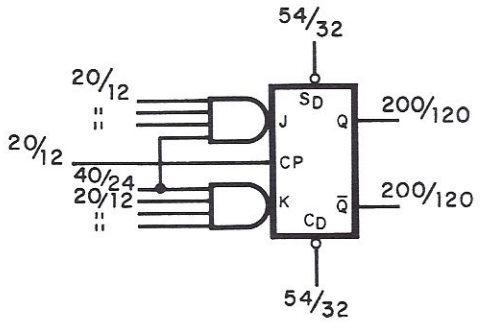


J-K FLIP-FLOPS

9000



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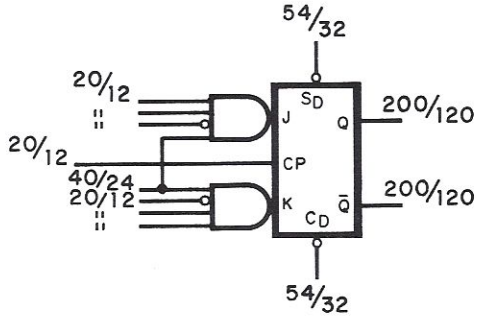
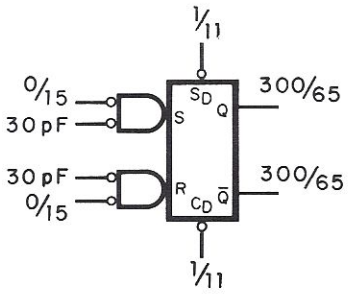


* See Note 1

CCSL INPUT LOAD & DRIVE FACTORS

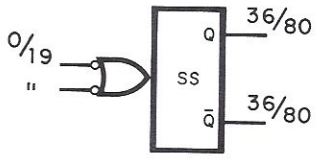
BINARY

9950



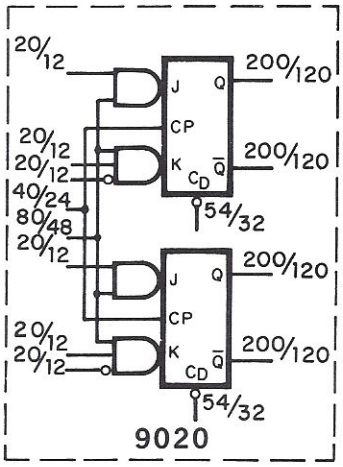
ONE-SHOTS (MONOSTABLE)

9941 & 9951



DUAL FLIP-FLOPS

9020



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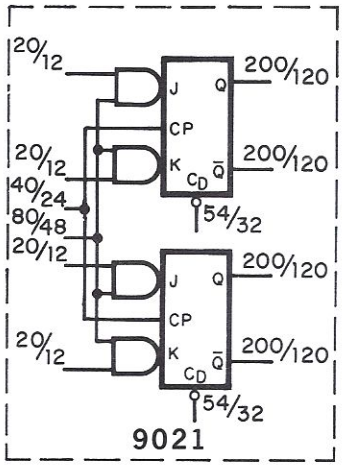

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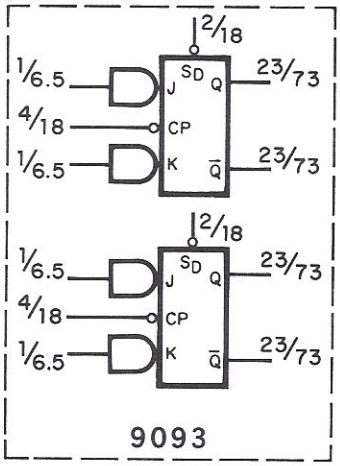

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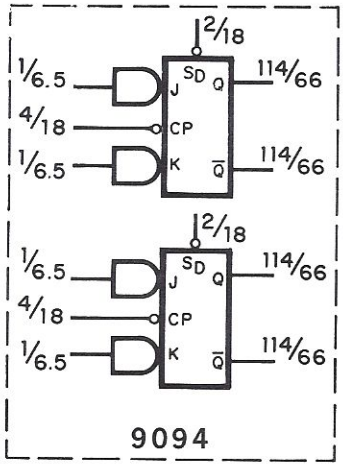

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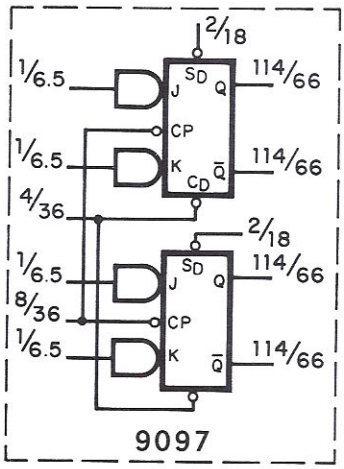

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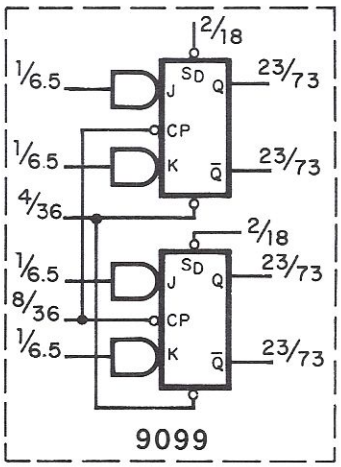
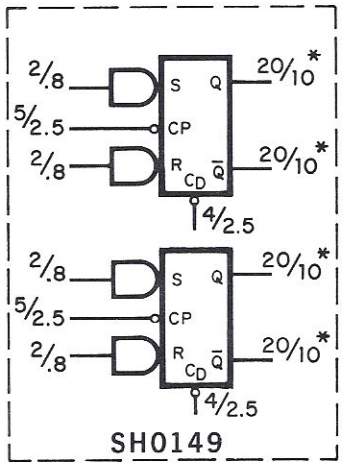
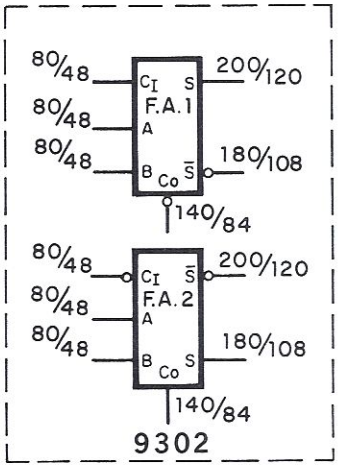


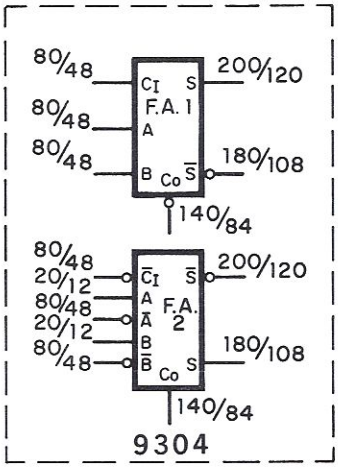
CCSL INPUT LOAD & DRIVE FACTORS

DUAL FLIP-FLOPS (continued)



DUAL FULL-ADDERS





OUTPUT LEVELS VERSUS LOADING

GATE TYPE ELEMENTS

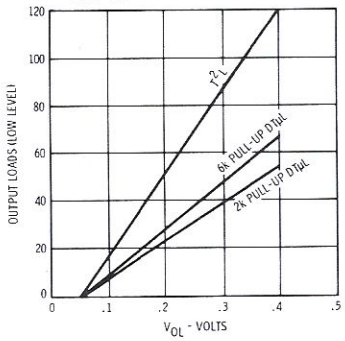


FIG. 1

BUFFER ELEMENTS

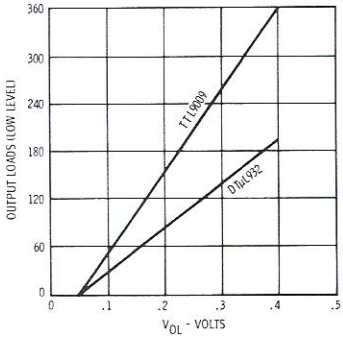


FIG. 2

6k PULL-UP

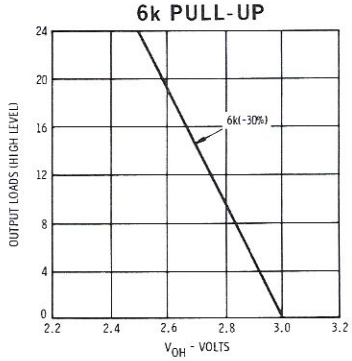


FIG. 3

2k PULL-UP

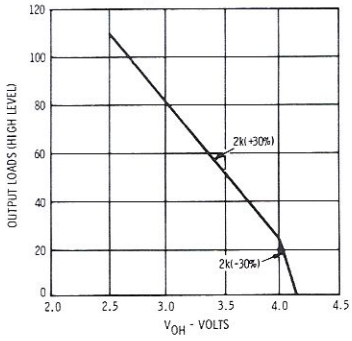


FIG. 4

* See Note 1

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